Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-6. (Canceled).

7. (Currently Amended) A method of data processing using a processor comprising a reconfigurable field of data processing cells ~~and a register, wherein the register has a data stream memory operated as a First-In-First-Out (FIFO) memory to store at least one data vector and wherein the reconfigurable field of data processing cells are interconnected by a reconfigurable multi-dimensional bus structure that includes dynamically allocatable bus resources that are sharable over a plurality of configurations and that are configured for transmitting data directly from any one of the data processing cells to any other of the data processing cells~~, the method comprising: ~~providing a program corresponding to a sequence of compilable high-level language instructions; determining, for the reconfigurable field of data processing cells, a set of configurations of the reconfigurable field of data processing cells, with respect to at least one of a function and an interconnection of the reconfigurable field of data processing cells, with execution of which configurations the program is run; determining, by a software compiler and for each of the configurations, a respective maximum allowed execution runtime prior to lapse of which the respective configuration is uninterruptible, and in response to lapse of which the reconfigurable field of data processing cells is reconfigured with a different configuration; executing the configurations, the executing including (a)~~

configuring ~~functions of~~ at least a subset of the data processing cells for execution by the ~~, (b) configuring an interconnection of~~ at least the [[a]] subset of the data processing cells ~~, and (c) dynamically allocating resources~~ of an entire loop of a program, the ~~bus structure~~ program including a sequence of compilable high-level language instructions; [[and]]

during the ~~executing : storing~~ execution of the loop using the at least the subset of the data processing cells according to the configuration established by the configuring step, ~~in the data stream memory, at least one of the data stream and parts of the data stream; and for each configuration,~~ monitoring a [[the]] respective maximum allowed execution runtime of the configuration; and

responsive to determining in the monitoring step that ~~in order to interrupt processing with the configuration if~~ the respective maximum allowed execution runtime is exceeded, interrupting ~~; wherein at least one of: (a) a single function of~~ the ~~program is executed via sequential~~ execution ~~of a plurality~~ of the ~~set of configurations; and (b) for each of at least one of the set of configurations, a plurality of functions of the program are executed in sequence via execution of a single instance of the respective configuration~~ loop prior to its completion, wherein the interrupting includes reconfiguring one or more of the at least the subset of the data processing cells.

8. (Currently Amended) The method as recited in claim [[7]] 24, further comprising:

using at least one of: i) a register allocation device to allocate the register, and ii) a register releasing device to release the register.

9. (Previously Presented) The method as recited in claim 8, wherein the register allocation device is preserved over multiple reconfigurations of the reconfigurable field of data processing cells.

10. (Currently Amended) The method as recited in claim [[7]] 24, wherein the register is a Random Access Memory (RAM) cell.

11. (Currently Amended) The method as recited in claim [[7]] 24, wherein the program includes a multitask application, the method further comprising:

using the register:

to provide read and write access when a virtual FIFO dividing line is implemented; and

for execution of at least one of two different tasks of the multitask application.

12. (Currently Amended) The method as recited in claim [[7]] 24, further comprising:

using at least one memory unit as a stack and to indicate at least one of a stack underflow state and a stack overflow state.

13. (Previously Presented) The method as recited in claim 12, wherein the at least one of the underflow state and overflow state is of an operating system unit.

14. (Canceled).

15. (Currently Amended) The method as recited in claim [[7]] 24, wherein a watchdog is used to recognize an exceedance of each respective maximum allowed execution runtime.

16. (Previously Presented) The method as recited in claim 15, wherein any one of the configurations that exceeds its respective maximum allowed execution runtime is treated as illegal.

17. (Currently Amended) The method as recited in claim [[7]] 24, wherein any one of the configurations that exceeds its respective maximum allowed execution runtime is treated as illegal.

18. (Canceled).

19. (Currently Amended) The method as recited in claim [[7]] 24, wherein an operating system performs a predefined step in response to an exceedance by a configuration of the configuration's maximum allowed execution runtime.

20. (Currently Amended) The method as recited in claim [[7]] 24, wherein at least one of the configurations calls another of the configurations as a sub-routine.

21. (Previously Presented) The method as recited in claim 15, wherein a signal of the watchdog initiates a system trap.

22. (Previously Presented) The method as recited in claim 21, wherein, in response to the system trap, an operating system performs steps defined for a response to an invalid instruction.

23. (Currently Amended) A method of ~~data processing~~ using a processor comprising a reconfigurable field of data processing cells ~~and a register, wherein the register has a data stream memory operated as a First-In-First-Out (FIFO) memory to store at least one data vector and wherein the reconfigurable field of data processing cells are interconnected by a reconfigurable multi-dimensional bus structure that includes dynamically allocatable bus resources that are sharable over a plurality of configurations and that are configured for transmitting data directly from any one of the data processing cells to any other of the data processing cells~~, the method comprising:

modifying, by ~~providing~~ a processor executing a software compiler, a loop of a program, the program including ~~corresponding to~~ a sequence of compilable high-level language instructions, to generate a modified version of the program, wherein ~~; determining, for~~ the modifying ~~reconfigurable field of data processing cells, a set of configurations of the reconfigurable field of data processing cells, with respect to at least one of a function and an interconnection~~ of the loop includes inserting into the loop a maximum value condition that is based on ~~reconfigurable field of data processing cells, wherein an instruction of the program is executed using a plurality of the configurations, the reconfigurable field being reconfigured between the use of different ones of the plurality of configurations; determining, by a software compiler and for each of the configurations,~~ a ~~respective~~ maximum allowed execution runtime ~~prior to lapse~~ of a ~~which the respective~~ configuration ~~is uninterruptible; implementing the configurations; and during the implementing: configuring functions~~ of at least a subset of the data processing cells; ~~configuring an interconnection of at least a subset of the data processing cells; dynamically allocating resources of the bus structure; storing, in the data stream memory, at least one of the data stream and parts of the data stream;~~ and

~~for each configuration, monitoring the respective maximum allowed execution runtime in order to interrupt processing with the configuration if the respective maximum allowed execution runtime is exceeded~~ outputting the modified version of the program.

24. (Currently Amended) A method of data processing using a processor comprising a reconfigurable field of data processing cells and a register, wherein the register has a data stream memory operated as a First-In-First-Out (FIFO) memory to store at least one data vector ~~and wherein the reconfigurable field of data processing cells are interconnected by a reconfigurable multi-dimensional bus structure that includes dynamically allocatable bus resources that are sharable over a plurality of configurations and that are configured for transmitting data directly from any one of the data processing cells to any other of the data processing cells~~, the method comprising:

providing a program corresponding to a sequence of compilable high-level language instructions;

determining, for the reconfigurable field of data processing cells, a set of configurations of the reconfigurable field of data processing cells, with respect to at least one of a function and an interconnection of the reconfigurable field of data processing cells, with execution of which configurations the program is run, wherein, for each of at least one of the configurations, a plurality of instructions of the program are executable via a single instance of the respective configuration;

determining, by a software compiler and for each of the configurations, a respective maximum allowed execution runtime prior to lapse of which the respective configuration is uninterruptible;

executing the configurations; and

during the executing:

configuring functions of at least a subset of the data processing cells;

configuring an interconnection of at least a subset of the data processing cells;

dynamically allocating resources of the bus structure;

storing, in the data stream memory, at least one of the data stream and parts of the data stream; and

for each configuration, monitoring the respective maximum allowed execution runtime in order to interrupt processing with the configuration if the respective maximum allowed execution runtime is exceeded.

25. (New) A method of data processing using a processor comprising a reconfigurable field of data processing cells, the method comprising:

configuring, by the processor, a first subset of the data processing cells, such that the first subset of the data processing cells has a first configuration while one or more other subsets of the data processing cells has, respectively, one or more other configurations;

processing data, by the first subset of the data processing cells, while the first subset of the data processing cells is configured with the first configuration;

monitoring, by the processor, whether a maximum allowed execution runtime of the first configuration is exceeded; and

responsive to determining, in the monitoring step, that the maximum allowed execution runtime of the first configuration is exceeded, removing, by the processor, the first configuration and the one or more other configurations.

26. (New) The method of claim 25, where the maximum allowed execution runtime of the first configuration is determined by the processor to be exceeded conditional upon a lapse of the maximum allowed execution runtime without the first subset of the data processing cells requesting a new configuration.

27. (New) The method of claim 25, wherein the first subset of the data processing cells is adapted to, while the first subset of the data processing cells is configured with the first configuration, request a new configuration of one or more of the first subset of the data processing cells.

28. (New) The method of claim 23, further comprising;

executing, by the at least the subset of the data processing cells, the modified loop while configured according to the configuration.

29. (New) A method of data processing using a processor comprising a reconfigurable field of data processing cells, the method comprising:

while the field is configured with a first configuration, triggering, with the first configuration, extraction of an entry from a stack and transmission of the entry as a call for reconfiguration.

30. (New) The method of claim 29, further comprising:

while the field is configured with a second configuration, and prior to the configuration of the field with the first configuration, entering, with the second configuration, the entry into the stack.

31. (New) The method of claim 30, wherein the configuration of the field to have the first configuration is triggered with the second configuration.

32. (New) A method of data processing using a processor comprising a reconfigurable field of data processing cells and a memory arrangement, wherein the memory arrangement stores therein a data vector, the method comprising:

sequentially reading, by the field using a first configuration of the field, a first subset of data elements of the data vector;

monitoring whether a maximum allowed execution runtime of the first configuration is exceeded;

responsive to determining in the monitoring step that the maximum allowed execution runtime is exceeded, removing the first configuration and configuring the field with a second configuration prior to readout of all of the data elements of the data vector, such that a second subset of the data elements of the data vector remains unread in the memory arrangement; and

subsequent to the removing of the first configuration and the configuring of the field with the second configuration, sequentially reading, by the field using the second configuration, one or more data elements of the second subset of the data elements.

33. (New) The method of claim 32, further comprising:

for each of the sequentially read data elements, updating a pointer to point to a different memory location of the memory arrangement than prior to the updating, wherein a beginning of the sequential reading of the one or more data elements of the second subset of the data element is performed based on a position into which the pointer entered while the field was configured with the first configuration.